IN THE CLAIMS

Please amend the claims as follows:

1. (currently amended) An apparatus for providing bus arbitrations in a multiprocessor system, said apparatus comprising:

a bus request history table for storing a history of bus requests for a system bus made by a plurality of cores, wherein said bus request history table includes a current sequence number column, a processor sequence column, a next sequence number column, and a number of misses column, wherein said system bus is shared by said plurality of cores; and

an arbiter, coupled to said bus request history table, for arbitrating said system bus among said plurality of cores in response to bus requests made by said plurality of cores, according to information stored in said bus request history table.

2. (original) The apparatus of Claim 1, wherein said bus request history table includes a current bus owner column, a next bus owner column, and a number of misses column.

3. (original) The apparatus of Claim 2, wherein said arbiter, in response to a bus request from a core having an entry in said current bus owner column, automatically grants said system bus to a core according to a corresponding entry in said next bus owner column after said bus request.

4. (original) The apparatus of Claim 2, wherein said bus request history table is implemented by a cache memory.

Please cancel Claim 5.

6. (original) The apparatus of Claim 5, wherein said arbiter, in response to bus requests from a sequence of cores having an entry in said processor sequence column, automatically grants said system bus to a sequence of cores according to a corresponding entry in said next sequence number column after said bus requests.

7. (original) The apparatus of Claim 5, wherein said bus request history table is implemented by content-addressable memory.

8. (original) The apparatus of Claim 1, wherein said core is a processor.

9. (currently amended) A method for providing bus arbitrations in a multiprocessor system, said method comprising:

storing a history of bus requests for a system bus made by a plurality of cores in a bus request history table, wherein said bus request history table includes a current sequence number column, a processor sequence column, a next sequence number column, and a number of misses column, wherein said system bus is shared by said plurality of cores; and

in response to bus requests made by said plurality of cores, arbitrating said bus requests according to information stored in said bus request history table.

10. (original) The method of Claim 9, wherein said bus request history table includes a current bus owner column, a next bus owner column, and a number of misses column.

11. (original) The method of Claim 10, wherein said arbitrating further includes automatically grants said system bus to a core according to a corresponding entry in said next bus owner column after said bus request, in response to a bus request from a core having an entry in said current bus owner column.

12. (original) The method of Claim 10, wherein said bus request history table is implemented by a cache memory.

Please cancel Claim 13.

14. (original) The method of Claim 13, wherein said arbitrating further includes automatically grants said system bus to a sequence of cores according to a corresponding entry in said next sequence number column after said bus requests, in response to bus requests from a sequence of cores having an entry in said processor sequence column.

15. (original) The method of Claim 14, wherein said bus request history table is implemented by content-addressable memory.

16. (original) The method of Claim 9, wherein said core is a processor.